CLAIM AMENDMENTS

1. (Currently Amended) A current supply circuit ~~(100)~~ providing an output current corresponding to digital data ~~(D0 - D5)~~ of n bits (wherein n is an integer not less than 2), comprising:

a current driving device;

a current output node ~~(DL)~~ electrically connected ~~with~~ to a first power supply node ~~(11)~~ via ~~a~~ said current driving device ~~(23)~~ during current supply;

a current control circuit ~~(110)~~ provided between a second power supply node ~~(12)~~ and said current output node and receiving ~~said~~ digital data ~~for controlling~~, corresponding to ~~said~~ the digital data, ~~an amount of~~ for controlling current ~~on~~ flowing in a current path ~~established~~, including said current output node, between ~~said~~ the first and second power supply nodes during ~~said~~ the current supply; and

a voltage regulating circuit ~~(140, 150)~~ receiving ~~said~~ the digital data for forcing, after ~~said~~ the current supply starts, a change in voltage on said current output node based on ~~said~~ the digital data.

2. (Currently Amended) The current supply circuit according to claim 1, wherein said current driving device includes a field effect transistor ~~(23)~~ having a source and a drain electrically connected ~~with said~~ to the first power supply node ~~(11)~~ and said current output node ~~(DL)~~, respectively, and a gate, and the gate and drain of said field effect transistor are electrically connected during ~~said~~ the current supply.

3. (Currently Amended) The current supply circuit according to claim 1, wherein,

during ~~said~~ the current supply, the voltage on said current output node ~~(DL)~~ settles to a steady voltage ~~(Vst)~~ corresponding to a level of ~~said~~ the output current depending on characteristics of said current driving device ~~(23)~~, and

said voltage regulating circuit ~~(140, 150)~~ exchanges electric charge with said current output node ~~(DL)~~ to move the voltage on said current output node closer to ~~said~~ the steady voltage depending on ~~said~~ the digital data ~~(D0 - D5)~~.

4. (Currently Amended) The current supply circuit according to claim 1, wherein said voltage regulating circuit ~~(140, 150)~~ includes:

a precharge circuit ~~(140)~~ precharging, prior to supply of ~~said~~ the output current, said current output node ~~(DL)~~ to a predetermined voltage ~~(Vbf)~~; and

a precharge regulating circuit ~~(150)~~ exchanging, from initiation of ~~said~~ the current supply onward, electric charge corresponding to ~~said~~ the digital data ~~(D0 - D5)~~ with said current output node.

5. (Currently Amended) The current supply circuit according to claim 4, wherein

said precharge regulating circuit ~~(150)~~ includes n regulating units ~~provided~~ corresponding to the respective n bits ~~(D0 - D5)~~ of ~~said~~ the digital data, and

said n regulating units include:

n respective ~~n~~ capacitors ~~(C0 - C5)~~ charged by respective first to n-th voltages ~~(V0 - V5)~~ prior to the supply of ~~said~~ the output current; and

n respective ~~n~~ switching devices ~~(170 - 175)~~ provided between said n respective ~~n~~ capacitors and said current output node ~~(DL)~~, and each of said n switches turns on or off depending on one corresponding bit of ~~said~~ the digital data during ~~said~~ the current supply.

6. (Currently Amended) The current supply circuit according to claim 5, wherein,

during ~~said~~ the current supply, the voltage on said current output node ~~(DL)~~ settles to a constant voltage ~~(Vst)~~ corresponding to a level of ~~said~~ the output current depending on characteristics of said current driving device ~~(23)~~, and

~~said~~ the predetermined voltage ~~(Vbf)~~, ~~said~~ the first to n-th voltages, ~~(V0 - V5)~~ and capacitances ~~(C0 - C5)~~ of said n capacitors are designed, for each of at least one of the combinations of the n bits of ~~said~~ the digital data, based on ~~a~~ conservation of charge that reflects ~~said~~ the constant voltage between before and after at least one of said n switching devices ~~(170 - 175)~~, corresponding to ~~said~~ the n bits, is turned on.

7. (Currently Amended) The current supply circuit according to claim 1, wherein

said current control circuit ~~(110)~~ includes n constant-current supplies ~~(120 - 125)~~ ~~provided~~ corresponding to the respective n bits ~~(D0 - D5)~~ of ~~said~~ the digital data and connected in parallel to said current output node ~~(DL)~~, and

said n constant-current supplies generate, corresponding to ~~said~~ the n respective ~~n~~ bits, first to n-th currents ~~(I1, I2, I4, I8, I32)~~ between ~~said~~ the second power supply node ~~(12)~~ and said current output node.

8. (Currently Amended) The current supply circuit according to claim 7, wherein ~~said~~ the first to n-th currents ~~(I1, I2, I4, I8, I32)~~ are set in gradations in a power of 2

corresponding to a predetermined ~~weighing~~ weighting of the n bits ~~(D0 - D5)~~ of ~~said~~ the digital data.

9. (Currently Amended) A current supply circuit ~~(100#)~~ providing an output current corresponding to digital data ~~(D0 - D5)~~ of n bits (wherein n is an integer not less than 2), comprising:

a current driving device;

a current output node ~~(DL)~~ electrically connected to a first power supply node ~~(11)~~ via ~~a~~ said current driving device ~~(23)~~ during current supply;

a current control circuit ~~(110)~~ provided between a second power supply node ~~(12)~~ and said current output node and receiving ~~said~~ digital data ~~for controlling~~, corresponding to ~~said~~ the digital data, ~~an amount of~~ for controlling current ~~on~~ flowing in a current path ~~established~~, including said current ~~data line~~ output node, between ~~said~~ the first and second power supply nodes during ~~said~~ the current supply; and

a voltage regulating circuit ~~(140, 150)~~ receiving ~~said~~ the digital data for moving, prior to ~~said~~ the current supply, a voltage on said current output node closer to a voltage corresponding to ~~said~~ the digital data.

10. (Currently Amended) The current supply circuit according to claim 9, wherein, during ~~said~~ the current supply, the voltage on said current output node ~~(DL)~~ settles to a steady voltage ~~(Vst)~~ corresponding to a level of ~~said~~ the output current depending on characteristics of said current driving device ~~(23)~~, and

said voltage regulating circuit ~~(140, 150)~~ includes:

a precharge circuit ~~(140)~~ precharging, during a first period ~~(t0 - ta)~~, said current output node to a predetermined voltage ~~(Vbf)~~; and

a precharge regulating circuit exchanging, during a second period ~~(ta-t1)~~, following ~~said~~ the first period, electric charge corresponding to ~~said~~ the digital data ~~(D0 - D5)~~ with said current output node to move the voltage on said current output node ~~(DL)~~ closer to ~~said~~ the steady voltage.

11. (Currently Amended) A display device ~~(10) performing~~ producing a gray-scale display corresponding to image data ~~(D0 - D5)~~ of n bits (wherein n is an integer not less than 2), comprising:

a current supply circuit ~~(100)~~ for supplying a display current corresponding to ~~said~~ the image data;

a plurality of pixel circuits ~~(20)~~, each pixel circuit including a current-driven light-emitting device ~~(21)~~ providing a brightness corresponding to a supplied current and a pixel driving circuit ~~(22)~~ for supplying said current-driven light-emitting device with a current corresponding to ~~said~~ the display current; and

a current data line ~~(DL)~~ for conveying ~~said~~ the display current, which is provided by said current supply circuit, to said plurality of pixel circuits, wherein

said pixel driving circuit has a current driving device ~~(23)~~ connected between said current data line and a first power supply node ~~(11)~~ during a predetermined period in which ~~said~~ the display current is conveyed thereto, and supplies said current-driven light-emitting device with a current corresponding to ~~said~~ the display current conveyed during the predetermined period, and

said current supply circuit includes:

a current control circuit ~~(110)~~ provided between a second power supply node ~~(12)~~ and said current data line and receiving ~~said~~ the image data for controlling, corresponding to ~~said~~ the image data, ~~an amount of~~ current ~~on~~ flowing in a current path ~~established~~, including said current data line, between said first and second power supply nodes during supply of said display current; and

a voltage regulating circuit ~~(140, 150)~~ receiving said image data for forcing, after supply of said display current starts, a change in voltage on said current data line based on said image data.

12. (Currently Amended) The display device according to claim 11, wherein

said current control circuit ~~(110)~~ includes n constant-current supplies ~~(120 - 125) provided~~ corresponding to the n respective ~~n~~ bits ~~(D0 - D5)~~ of ~~said~~ the image data and connected in parallel to said current data line, and

said n constant-current supplies generate first to n-th currents ~~(I1, I2, I4, I8, I16, I32)~~ on said current data line based on ~~said~~ the n respective ~~n~~ bits.

13. (Currently Amended) The display device according to claim 11, wherein,

during the supply of ~~said~~ the display current, the voltage on said current data line ~~(DL)~~ settles to a steady voltage ~~(Vst)~~ corresponding to a level of ~~said~~ the display current depending on characteristics of said current driving device ~~(23)~~, and

said voltage regulating circuit ~~(140, 150)~~ includes:

a precharge circuit ~~(140)~~ precharging, prior to the supply of ~~said~~ the display current, said current data line to a predetermined voltage ~~(Vbf)~~; and

a precharge regulating circuit ~~(150)~~ exchanging, from initiation of the supply of ~~said~~ the display current onward, electric charge corresponding to ~~said~~ the image data with said current data line to move the voltage on said current data line closer to ~~said~~ the steady current.

14. (Currently Amended) The display device according to claim 13, wherein

said precharge regulating circuit ~~(150)~~ includes n precharge regulating units ~~provided~~ corresponding to the n respective ~~n~~ bits ~~(D0 - D5)~~ of ~~said~~ the image data, and said n precharge regulating units include:

n respective ~~n~~ capacitors ~~(C0 - C5)~~ charged by respective first to n-th voltages ~~(V0 - V5)~~ prior to the supply of ~~said~~ the display current; and

n respective ~~n~~ switching devices ~~(170 - 175)~~ provided between said n respective ~~n~~ capacitors and said current data line ~~(DL)~~, and each of said n switches turns on or off depending on one corresponding bit of ~~said~~ the image data during the supply of ~~said~~ the display current.